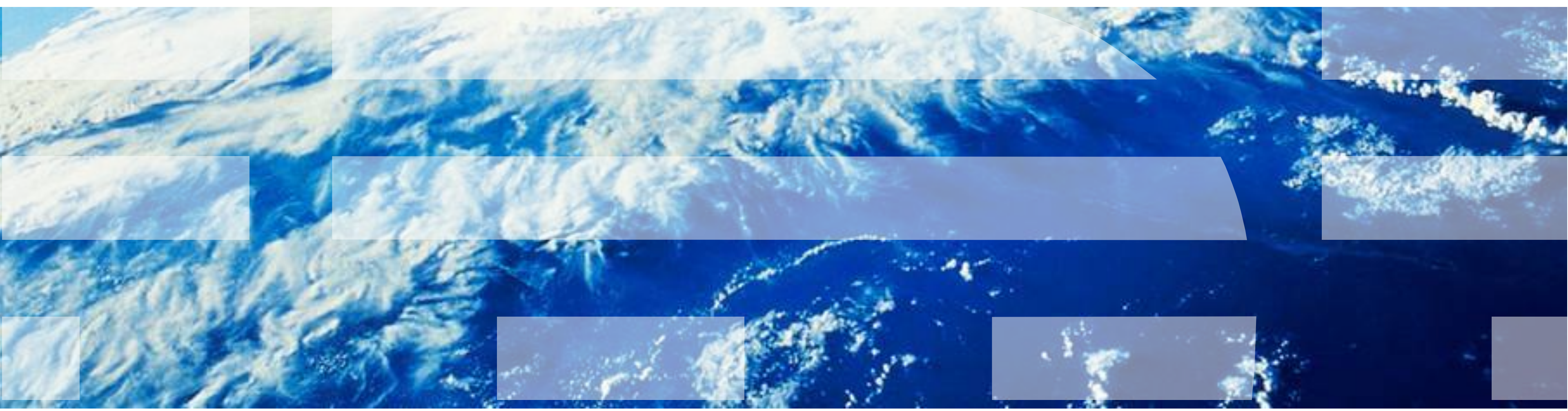
IBMの最新ハードウェアテクノロジーのご紹介

IBM Research Tokyo, Science & Technology,

Senior Manager

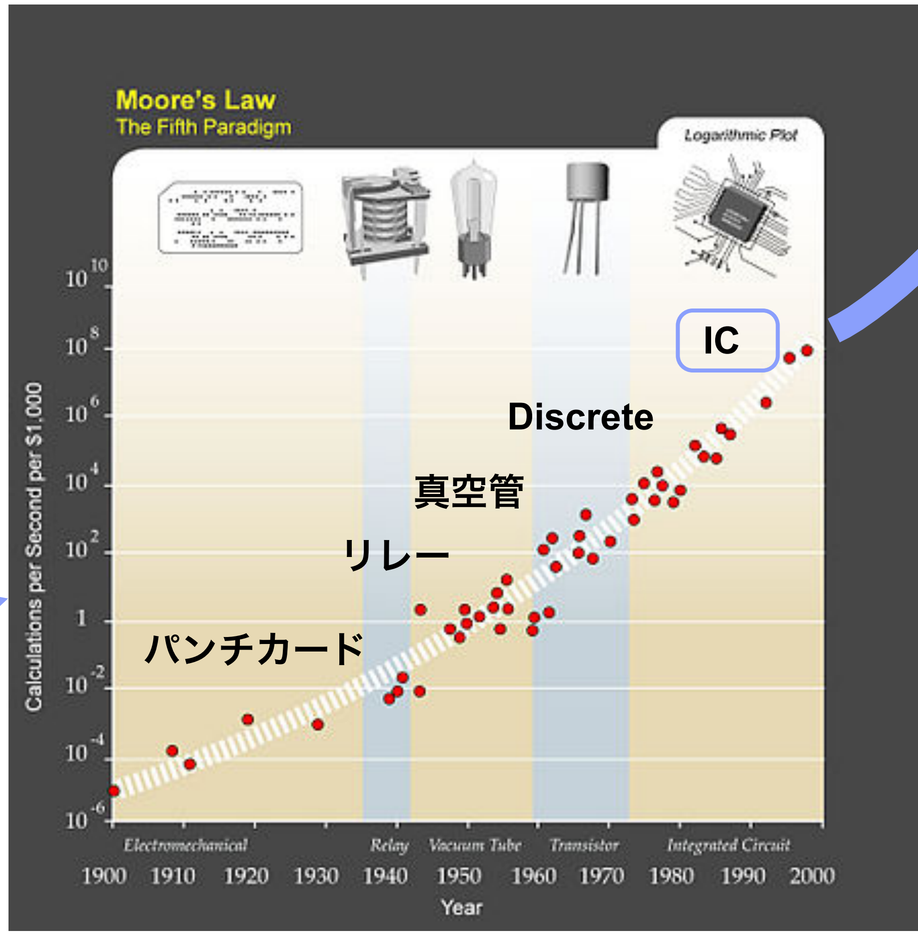
Shintaro Yamamichi, Ph. D.



Where we are

- 1990年: 「収穫加速の法則」by Ray Kurtzweil
  - **“Mooreの法則は、コンピュータ発展の 第5のパラダイム”**

1,000ドル・1秒当たりの計算能力



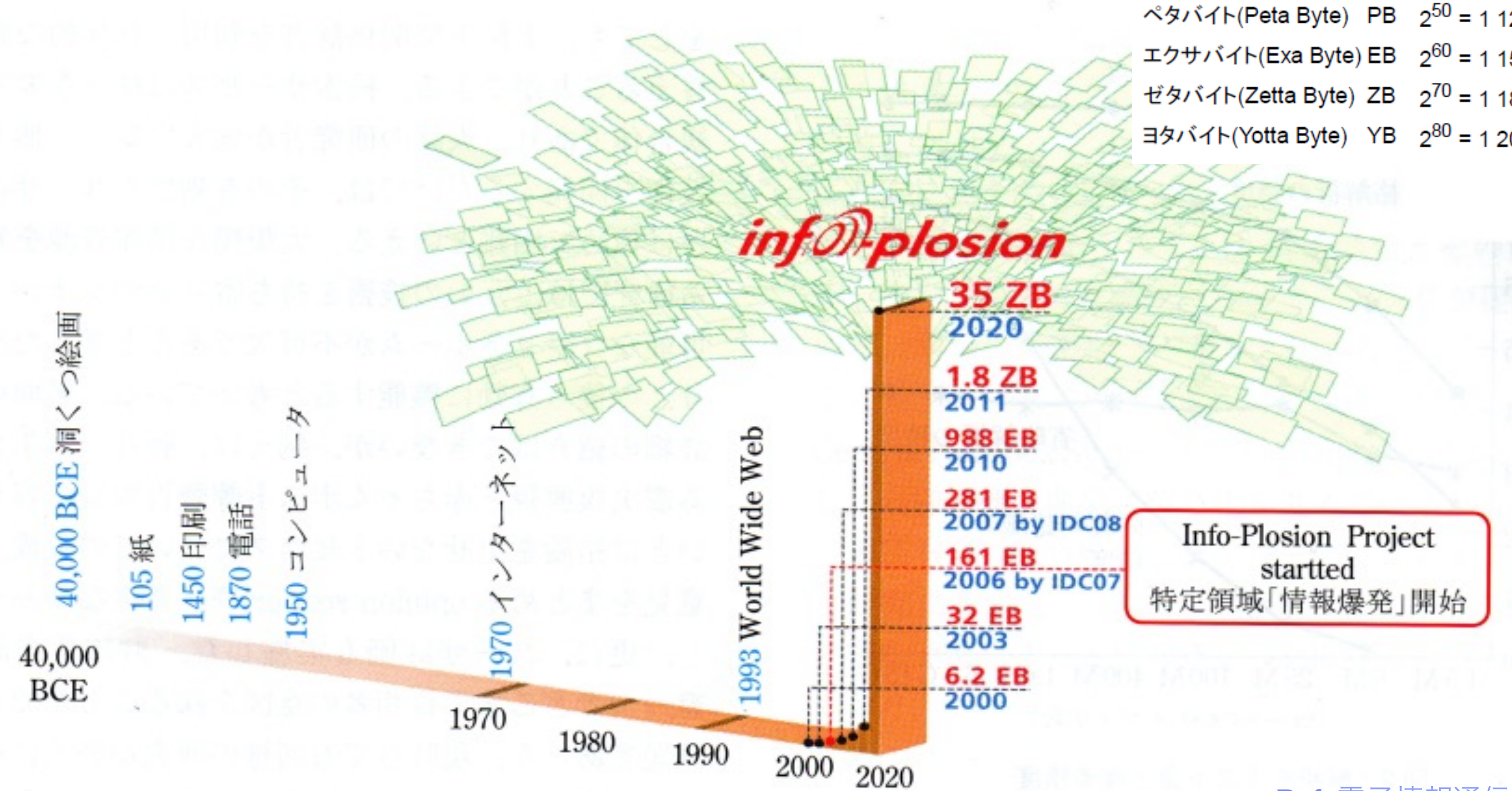
Wikipedia

What’s next?

情報爆発

- 1ZB (Zetta Byte) /年　@2010
  - 新聞朝刊(1MB)→約3.7兆年分

名前	記号	乗数
ビット(bit)	b	
キロバイト(Kilo Byte)	KB	2^{10} = 1 024
メガバイト(Mega Byte)	MB	2^{20} = 1 048 576
ギガバイト(Giga Byte)	GB	2^{30} = 1 073 741 824
テラバイト(Tera Byte)	TB	2^{40} = 1 099 511 627 776
ペタバイト(Peta Byte)	PB	2^{50} = 1 125 899 906 842 624
エクサバイト(Exa Byte)	EB	2^{60} = 1 152 921 504 606 846 976
ゼタバイト(Zetta Byte)	ZB	2^{70} = 1 180 591 620 717 411 303 424
ヨタバイト(Yotta Byte)	YB	2^{80} = 1 208 925 819 614 629 174 706 176



Ref. 電子情報通信学会誌
Vol.94,No.8,2011

データはさらに増え続ける

2012年

3

zettabytes

2020年

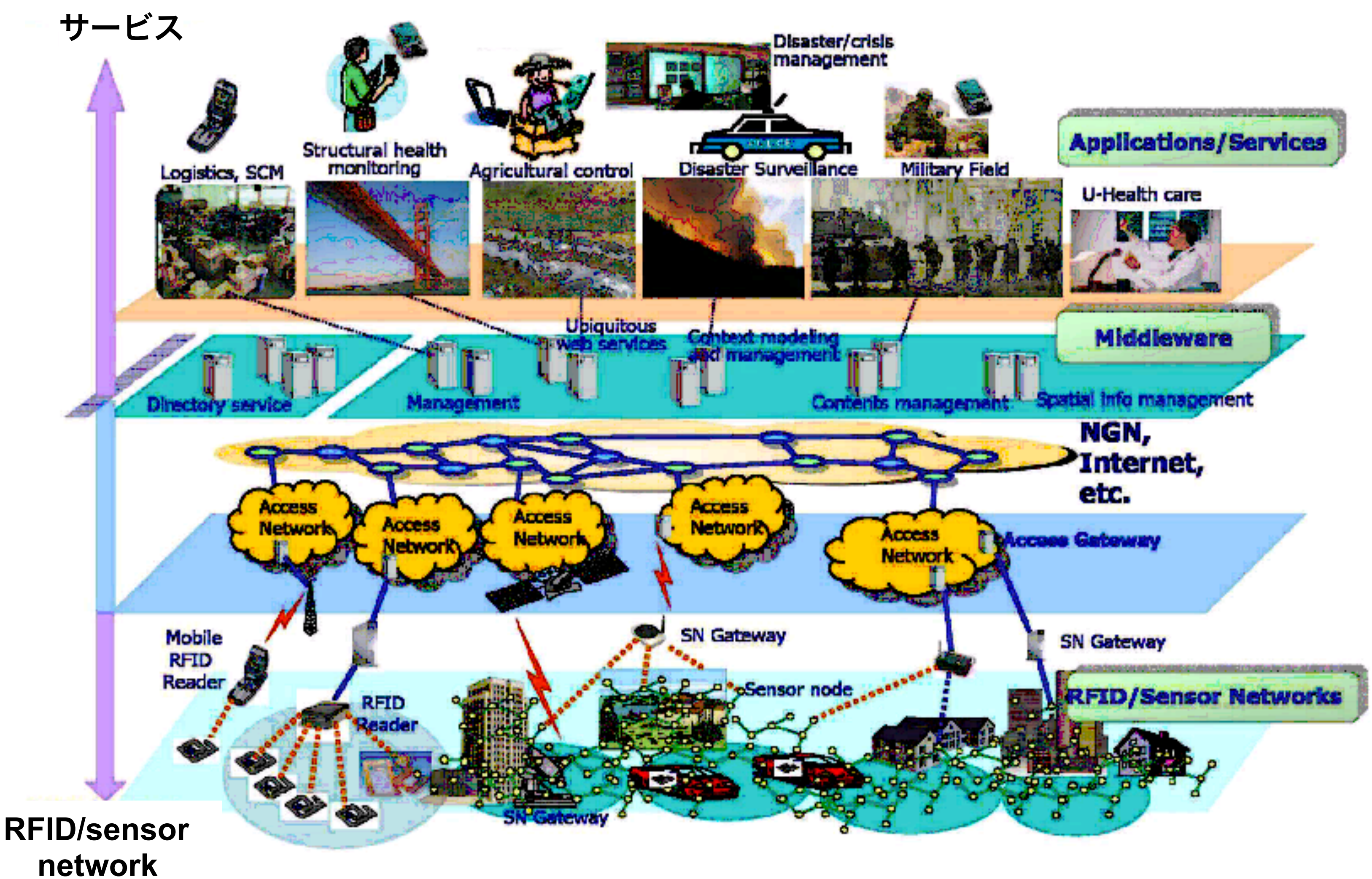
44

zettabytes

全世界で生み出されるデジタル情報の総量
500億本分の映画に相当

Source: IDC Digital Universe, IBM GTO 2015

Internet of Things



Internet of Things

あらゆるところでデータは生み出されている

2005年 **11%**

2020年 **42%**

全データにおけるセンサーデータの割合

Source: IDC Digital Universe

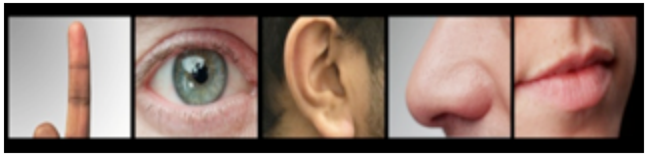
ヒトの脳のようなコンピューター

左脳

言語・会話・計算
概念・声や音の認知
論理的思考

右脳

五感
イメージ・図形・音楽
直感的思考



ITは第三世代へ

コグニティブ・システムの時代

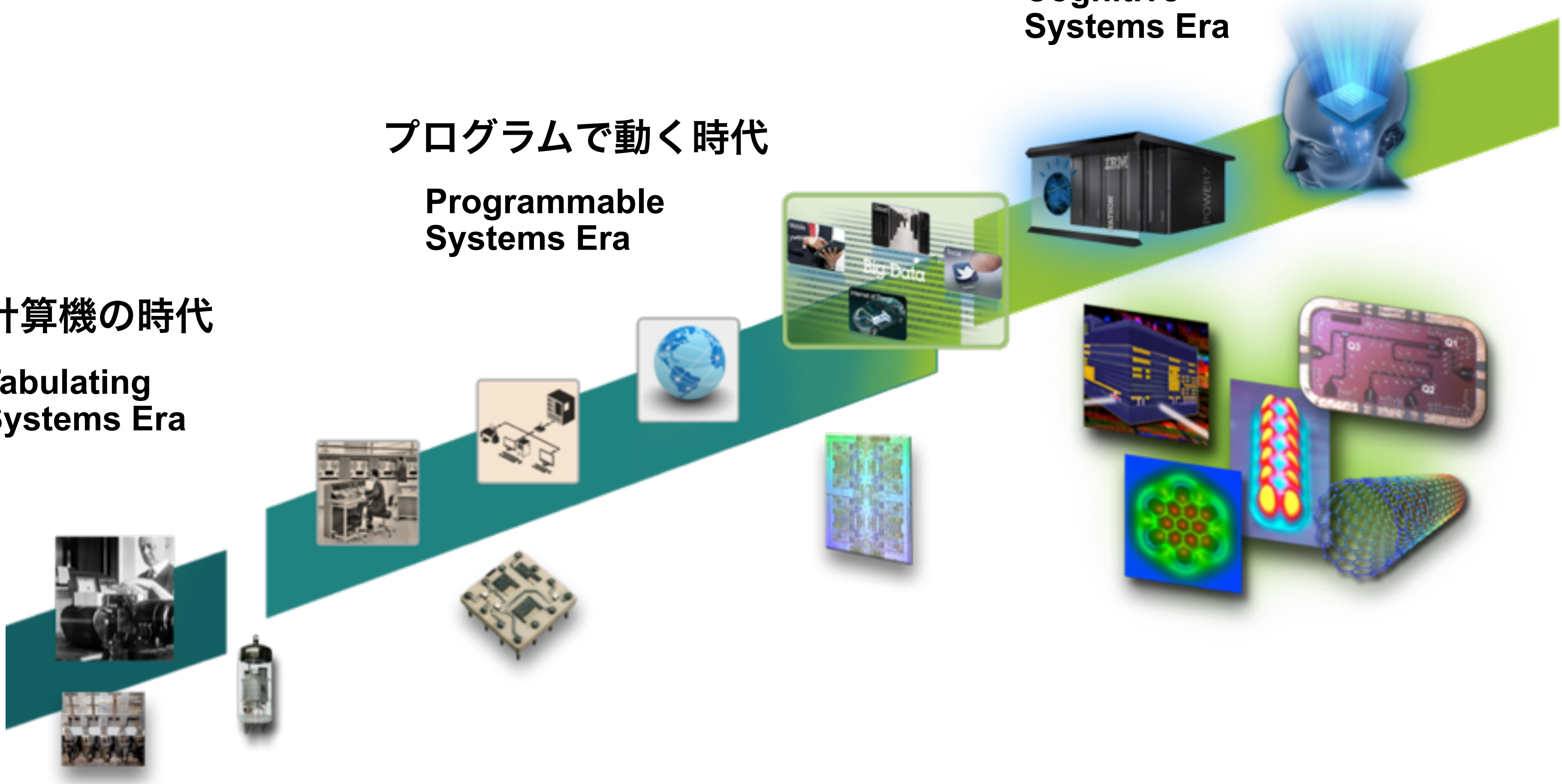
Cognitive Systems Era

プログラムで動く時代

Programmable Systems Era

計算機の時代

Tabulating Systems Era



コグニティブ・コンピューティングとは？

Cognition
In science, cognition is the set of all mental abilities and processes related to knowledge: attention, memory & working memory, judgment & evaluation, reasoning & "computation", problem solving & decision making, comprehension & production of language, etc.

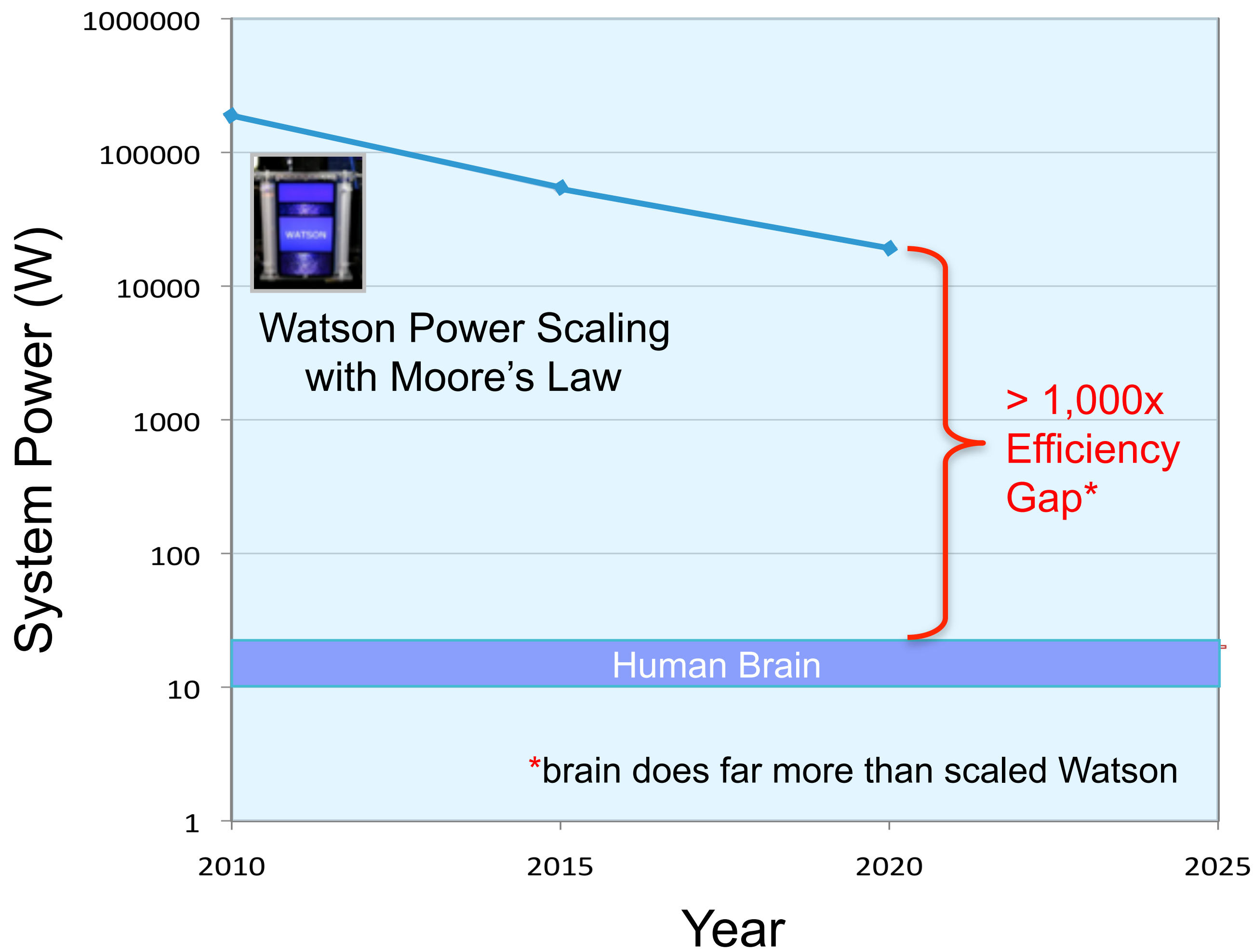
Cognitive Computer
A cognitive computer is a proposed computational device with a non-Von Neumann architecture that implements Hebbian learning.
非フォン・ノイマン型アーキテクチャー **ヘブ則**

人間の脳のように経験から学び、異なる事象間の関係性を見つけ、仮説を立て、判断し、記憶する機能を備えたコンピューターの概念

Source: Wikipedia / IBM

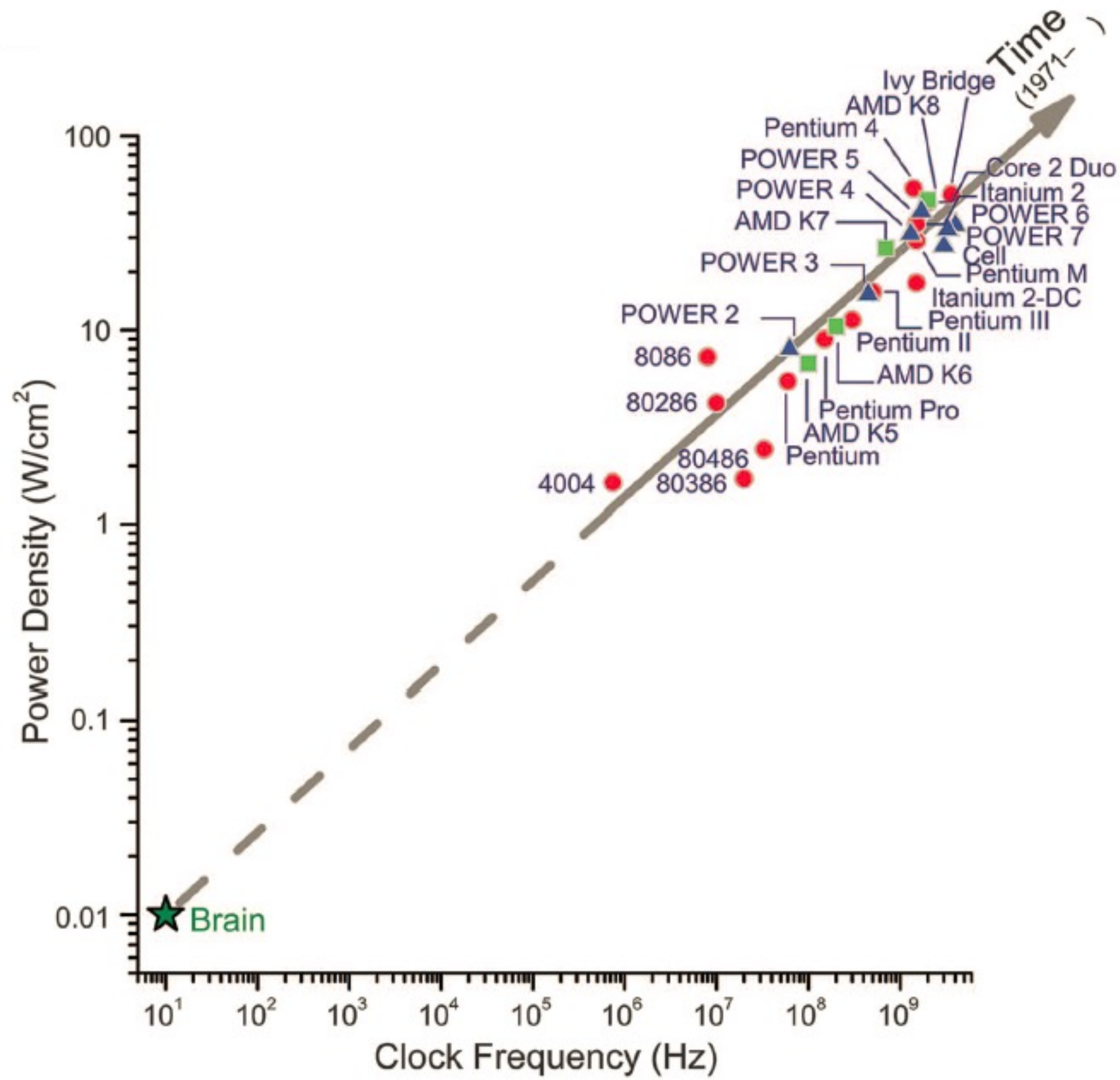
Watson vs. Brain

- Big efficiency gap calls for technology innovation



フォンノイマンアーキテクチャー vs 脳

IBM



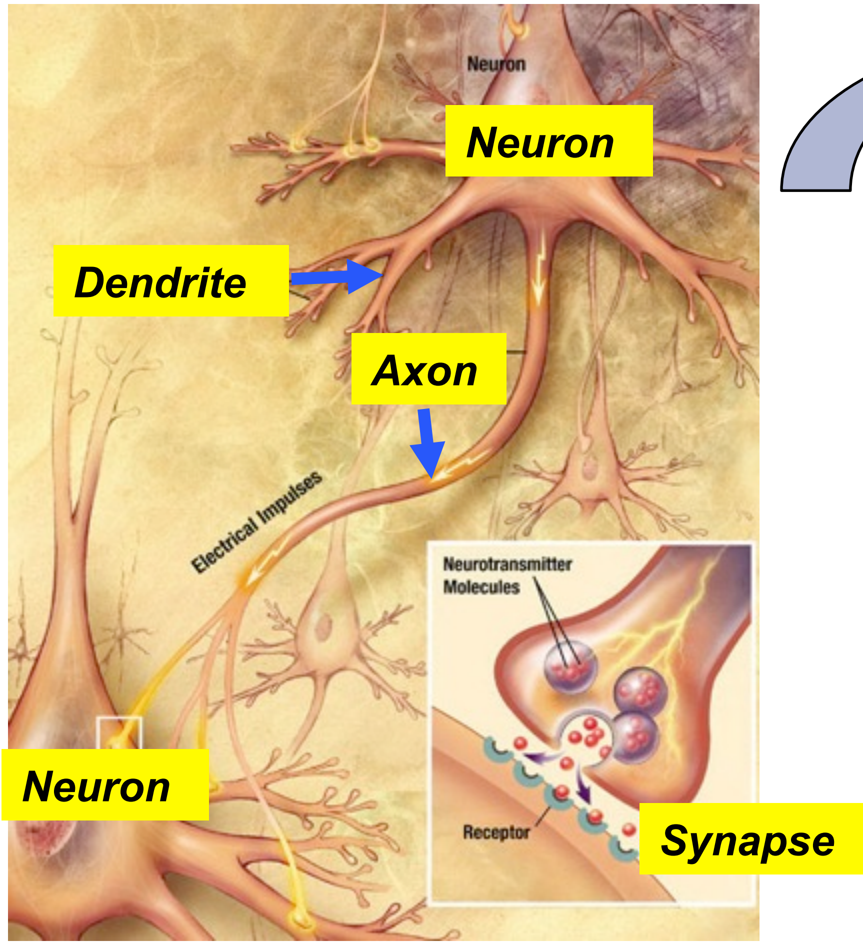
Dharmendra S. Modha
Science 345, pp668-673(2014)

コンピュータと脳は異質なデバイス

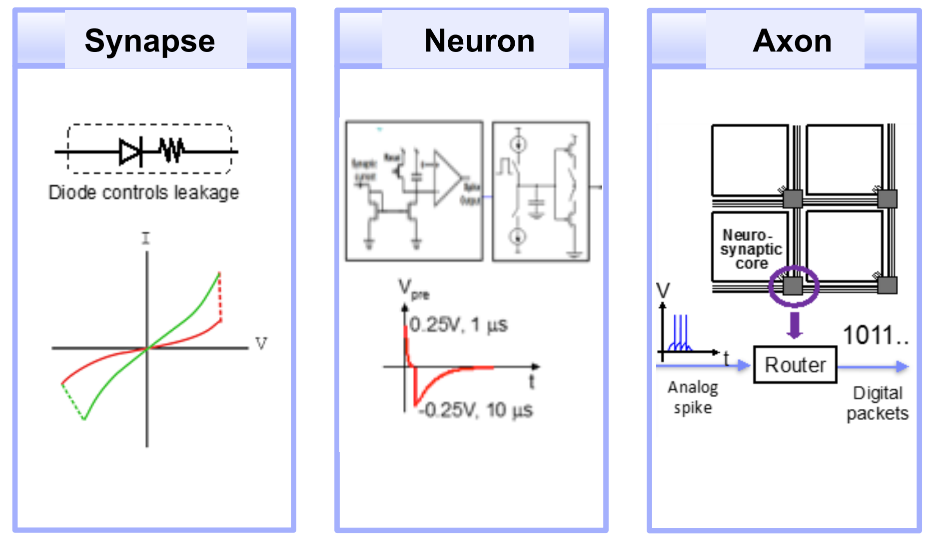
~5 GHz, sequential, linear	10 Hz, parallel, high fanout
200 kW	20 W
150um pitch, ~5K joints/cm^2	10um pitch, ~1M synapses/cm^2
CPU-バス-メモリシステム	CPU-メモリ共役システム

Neuromorphic Device

- Brain-Inspired device

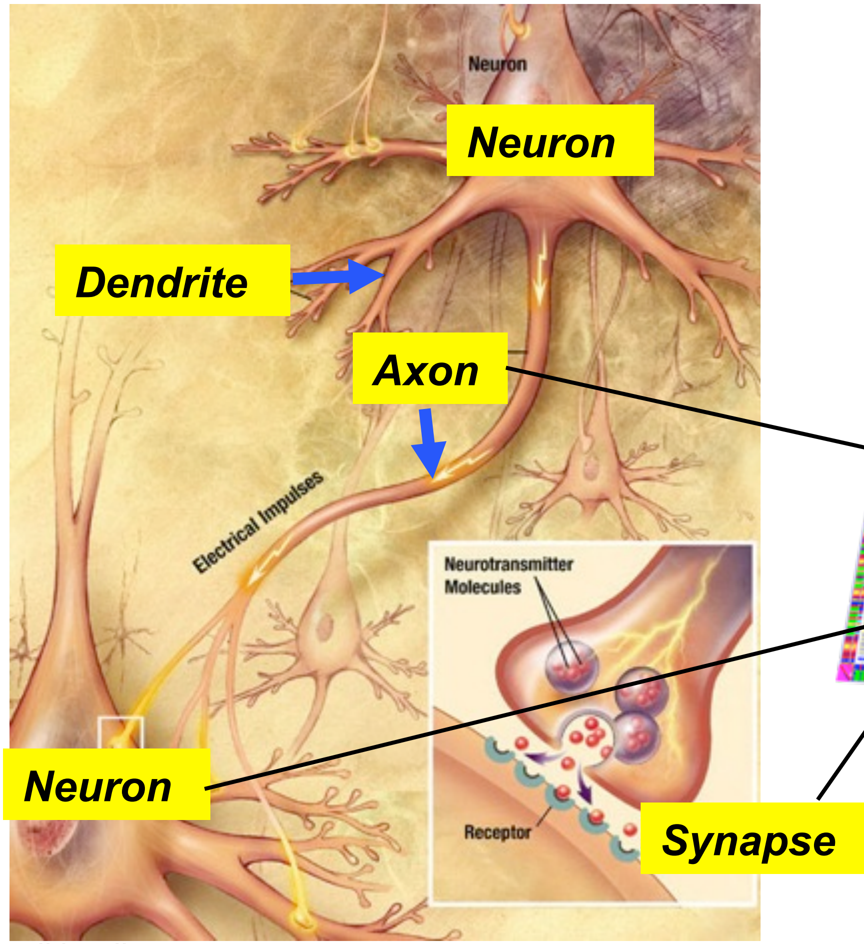


wikipedia



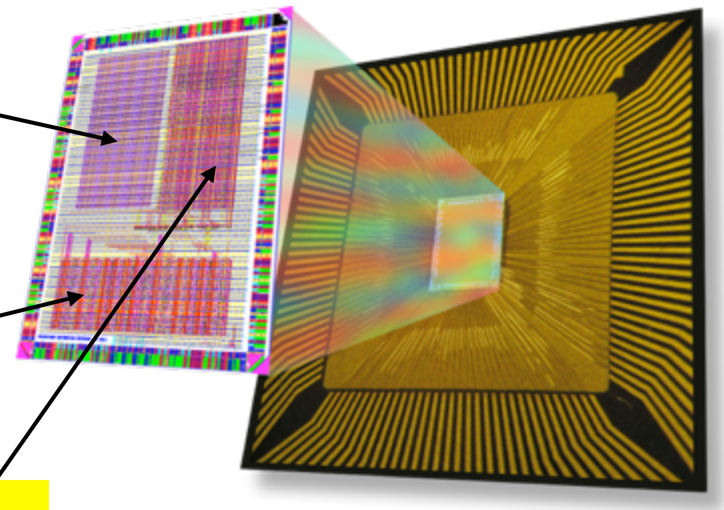
SyNAPSE chip

- SyNAPSE : *Systems of Neuromorphic Adaptive Plastic Scalable Electronics*



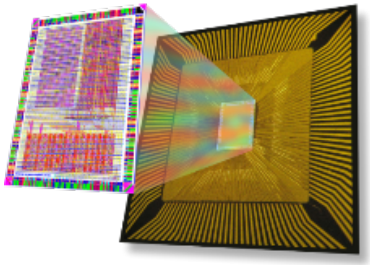
wikipedia

256 neurons, 256k synapses,
field-programmable
Merolla et al., 2011; Arthur et al., 2012



SyNAPSE 2nd Generation : “TrueNorth”

1st gen (2011)



<u>256 neurons</u>
260K synapses

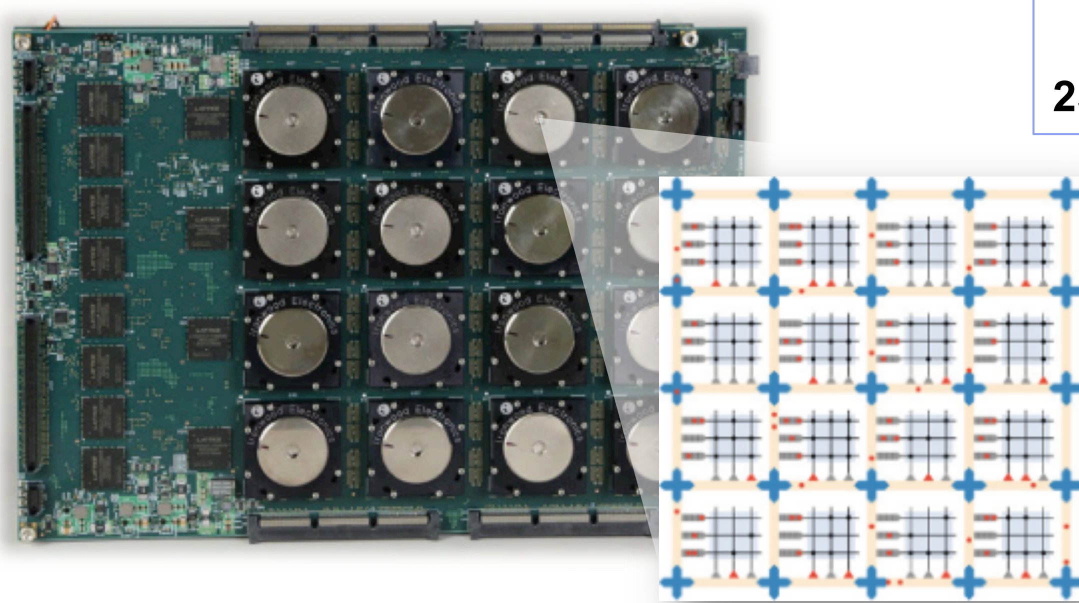
3.8M transistors
45pJ/spike

2nd gen (2014)

<u>1M neurons</u>
256M synapses

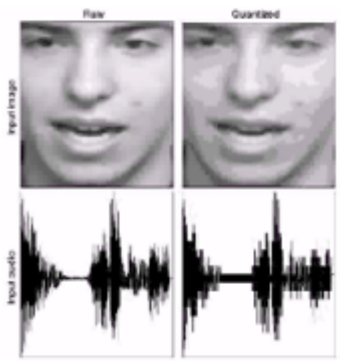
5.4B transistors
70mW (20mW/cm^2)

4096 Cores
1 Core
256 neurons
256 x 256 synapse
256 x 4096 = 1M neurons



8 August 2014

SyNAPSE "TrueNorth"

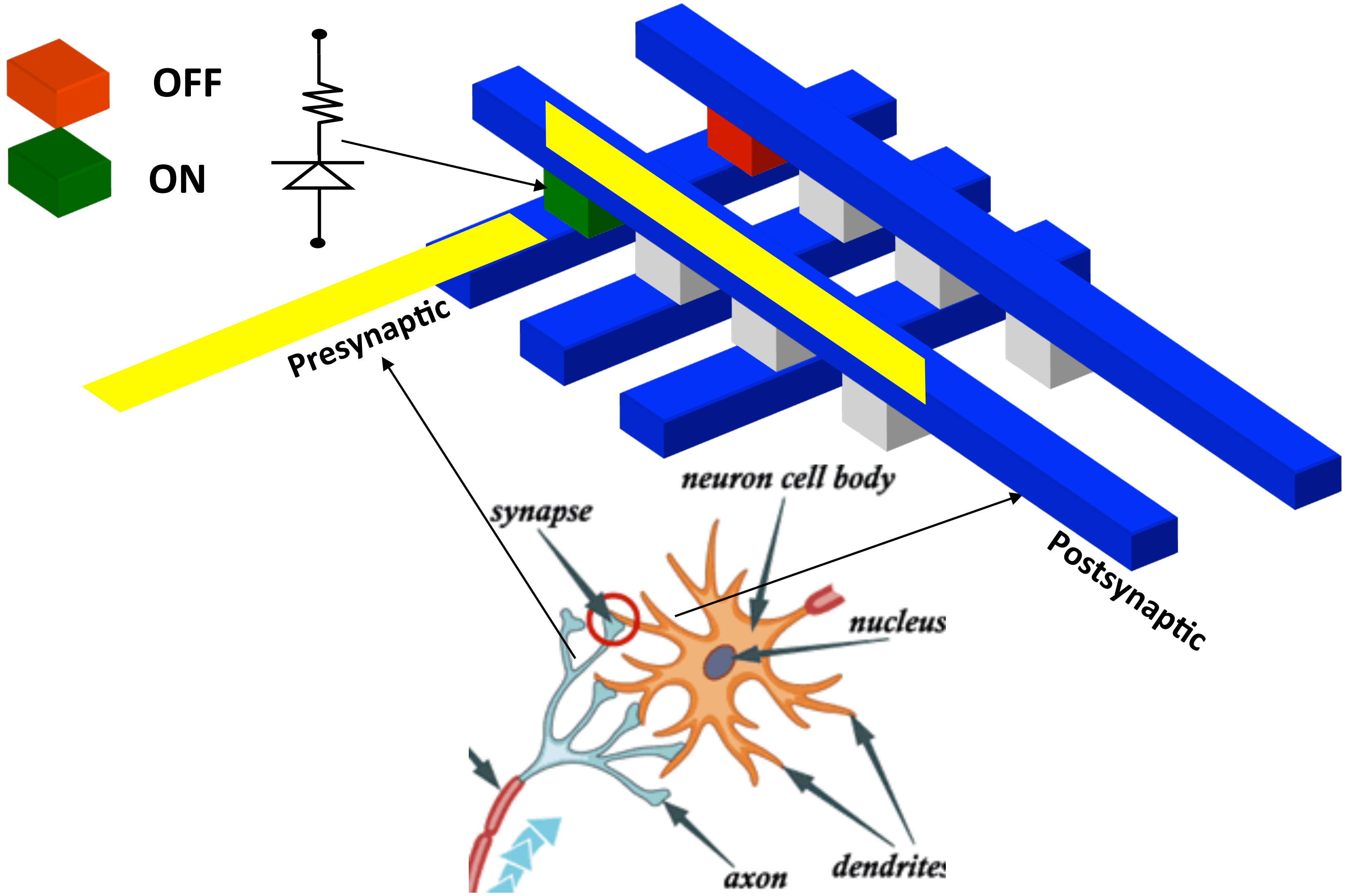


Speaker recognition by face image and voice

Handwriting recognition

Object recognition and tracking

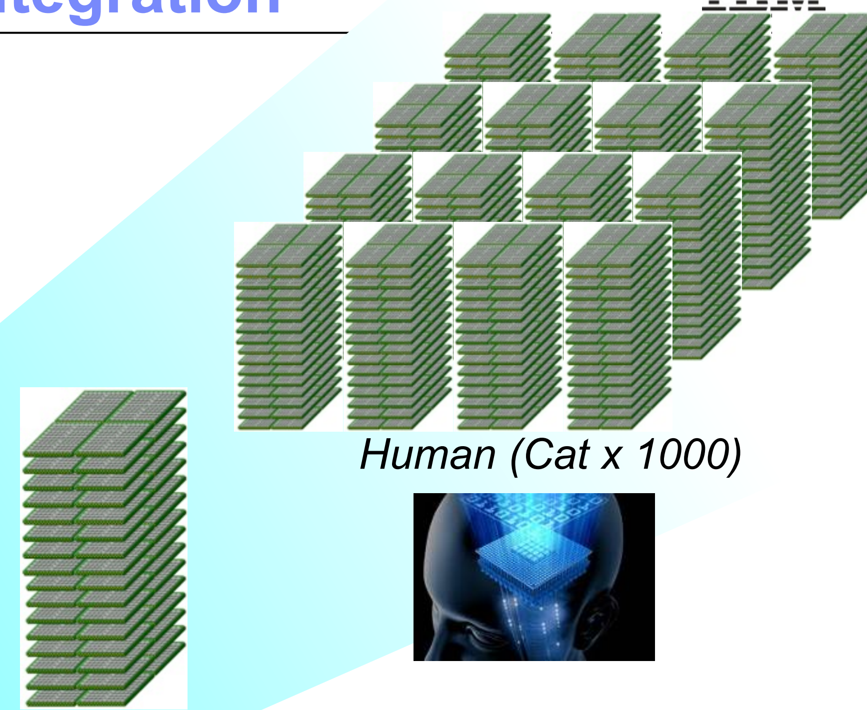
IBM Creating New Cognitive Technologies

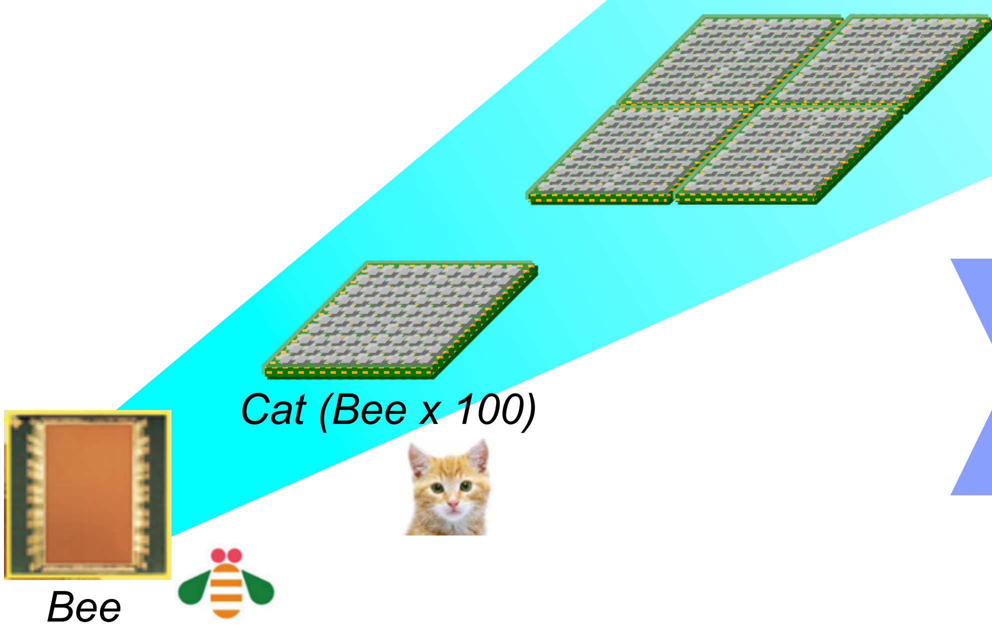


Power, space, memory, and communication scale with synapses

Challenges for Neuromorphic Integration

	Synapse	Neuron
SyNAPSE Chip x 1	256M	1M
Bee	8.5B	0.85M
SyNAPSE Chip x 100	25.6B	100M
Cat	1T	100M
SyNAPSE Chip x 100K	25.6T	100B
Human	1000T	100B



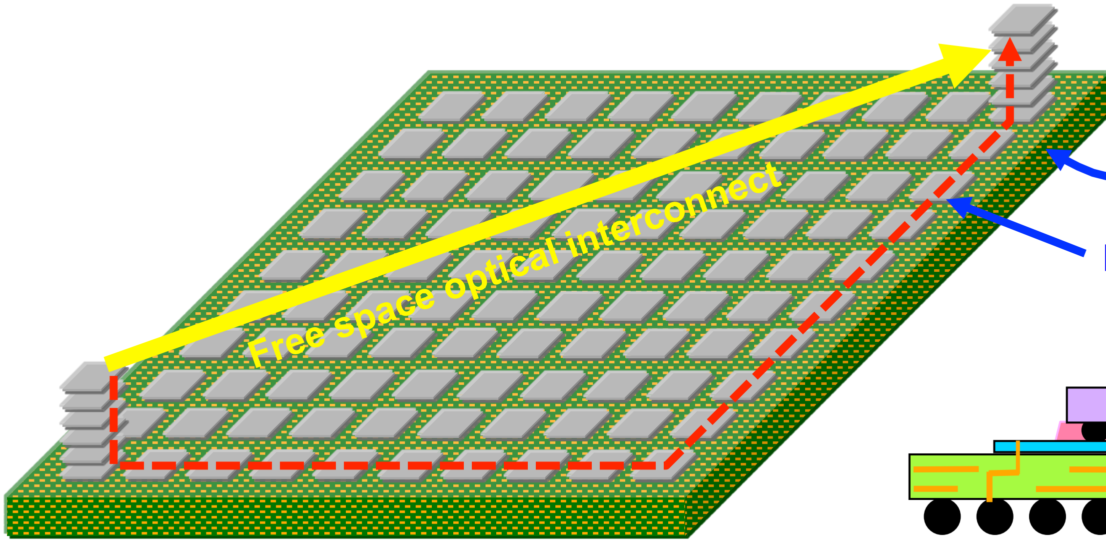


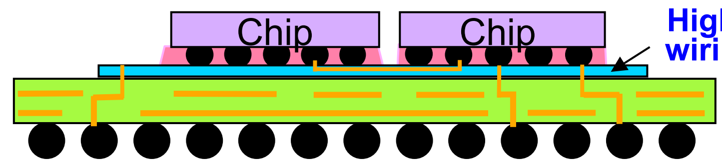
individual neuron research → synaptic integration research → axon interconnect research

"Axon" Innovation needed!

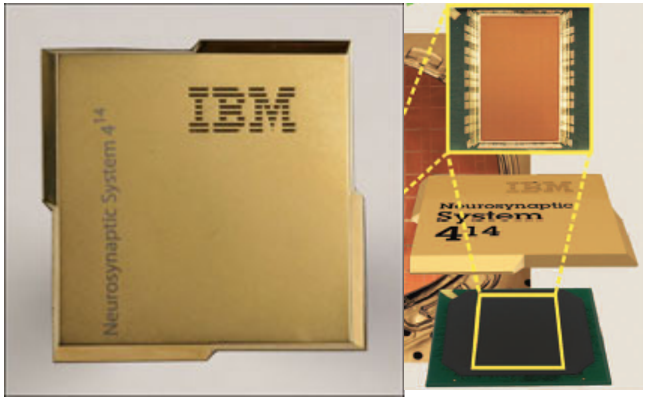
Neuromorphic Interconnection

- High density interconnection and 3D stacking for future scalable synaptic architecture



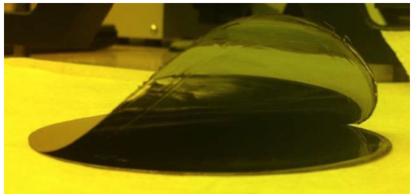


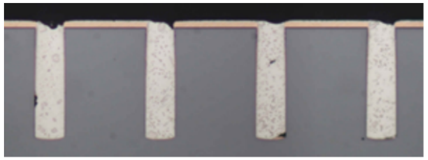
Interconnect bottle neck for synaptic architecture



TrueNorth module with 1M neurons

3D stacking



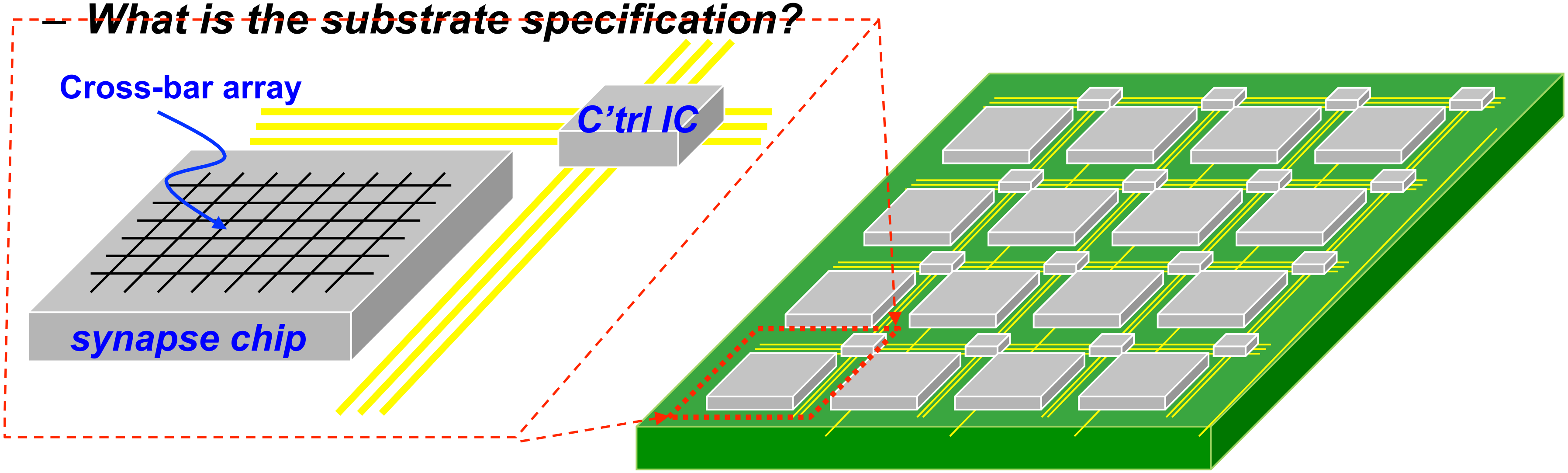


Low-cost TSV fill

Interposer challenges

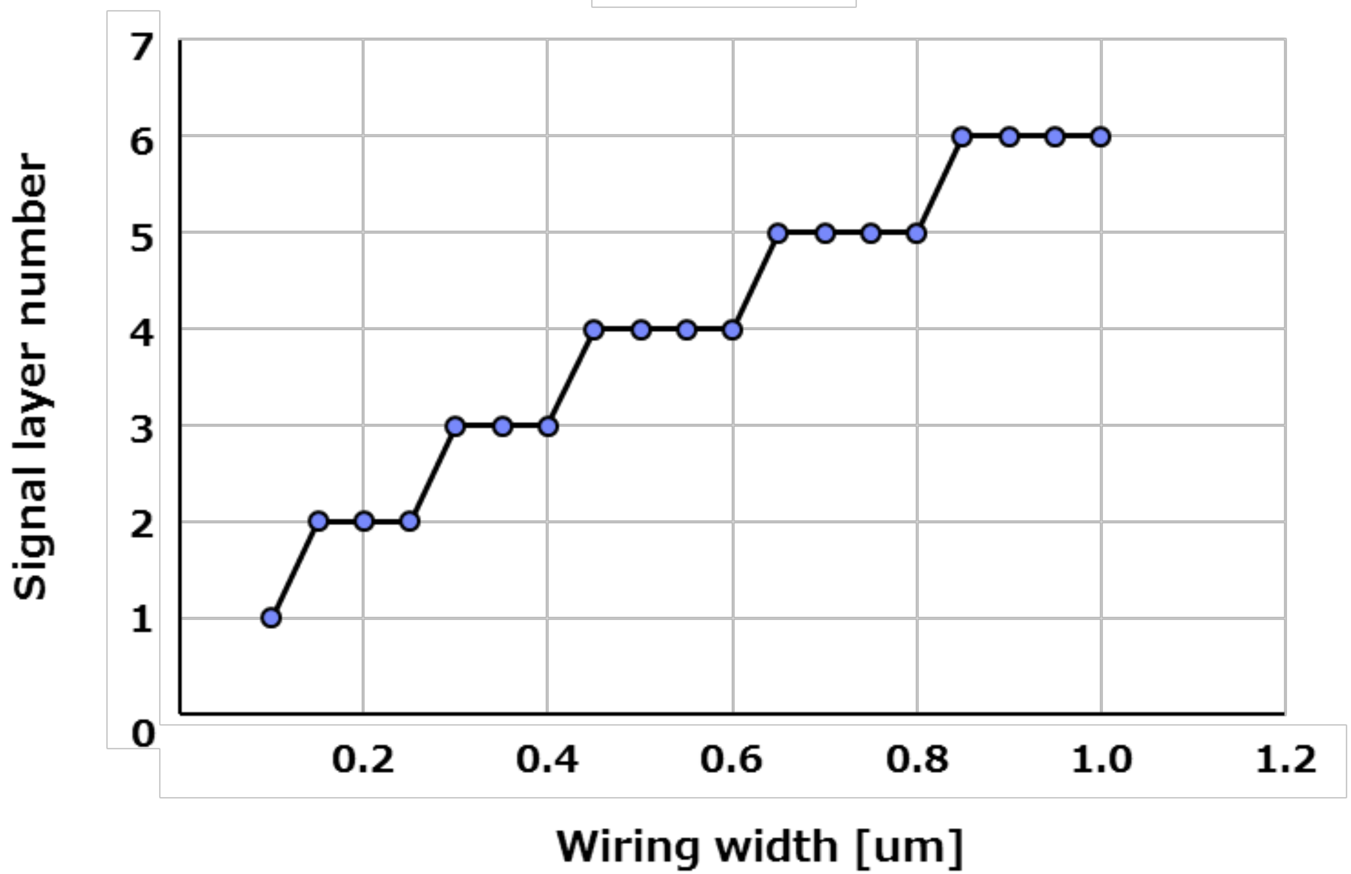
- Assumptions:
  - **0.7 M neurons & 7 B synapses :**
  - **2 chip configuration : 1 synapse chip & 1 controller IC**
    - **Synapse chip : cross-bar array type, 10 x 10 mm for 438 M sypanse**
      -> 16 chips required
    - **Controller IC : smaller**
  - **Packaging : 2.5D integration, all cross-points accessible**
    - **Chip to substrate interconnections : 10 um**

- Challenges :
  - ***What is the substrate specification?***



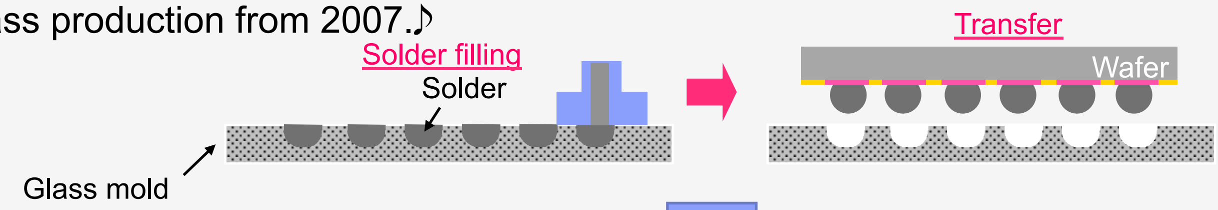
Interposer challenges

- Specifications:
  - **Wiring pitch : < 1.0 um !**
  - **Signal layers : 1 to 6 layers !**

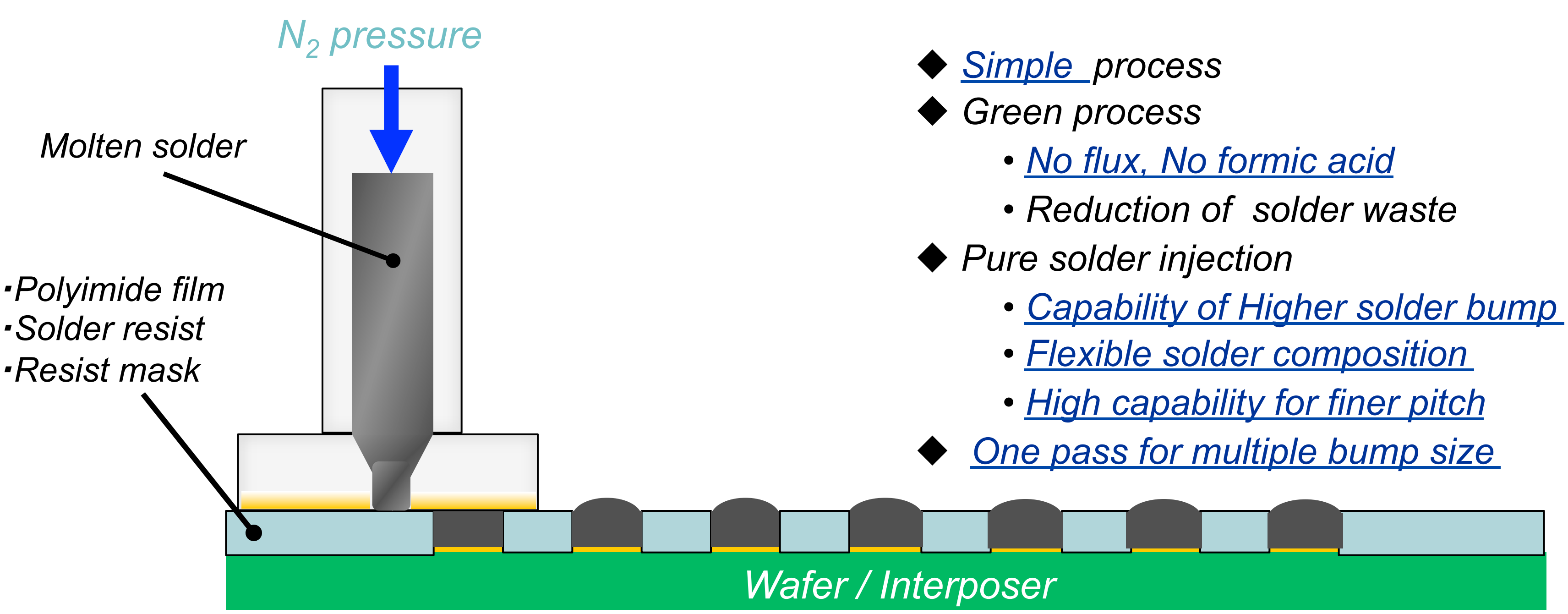


IMS (Injection Molded Solder)

- C4NP (C4 New Process) for wafer bumping
  - Adopted in IBM' mass production from 2007.♪



Solder filling + Transfer -> " 1process "



- ◆ *Simple process*
- ◆ *Green process*
  - *No flux, No formic acid*
  - *Reduction of solder waste*
- ◆ *Pure solder injection*
  - *Capability of Higher solder bump*
  - *Flexible solder composition*
  - *High capability for finer pitch*
- ◆ *One pass for multiple bump size*

Bump structure formed by IMS with different Cu thickness

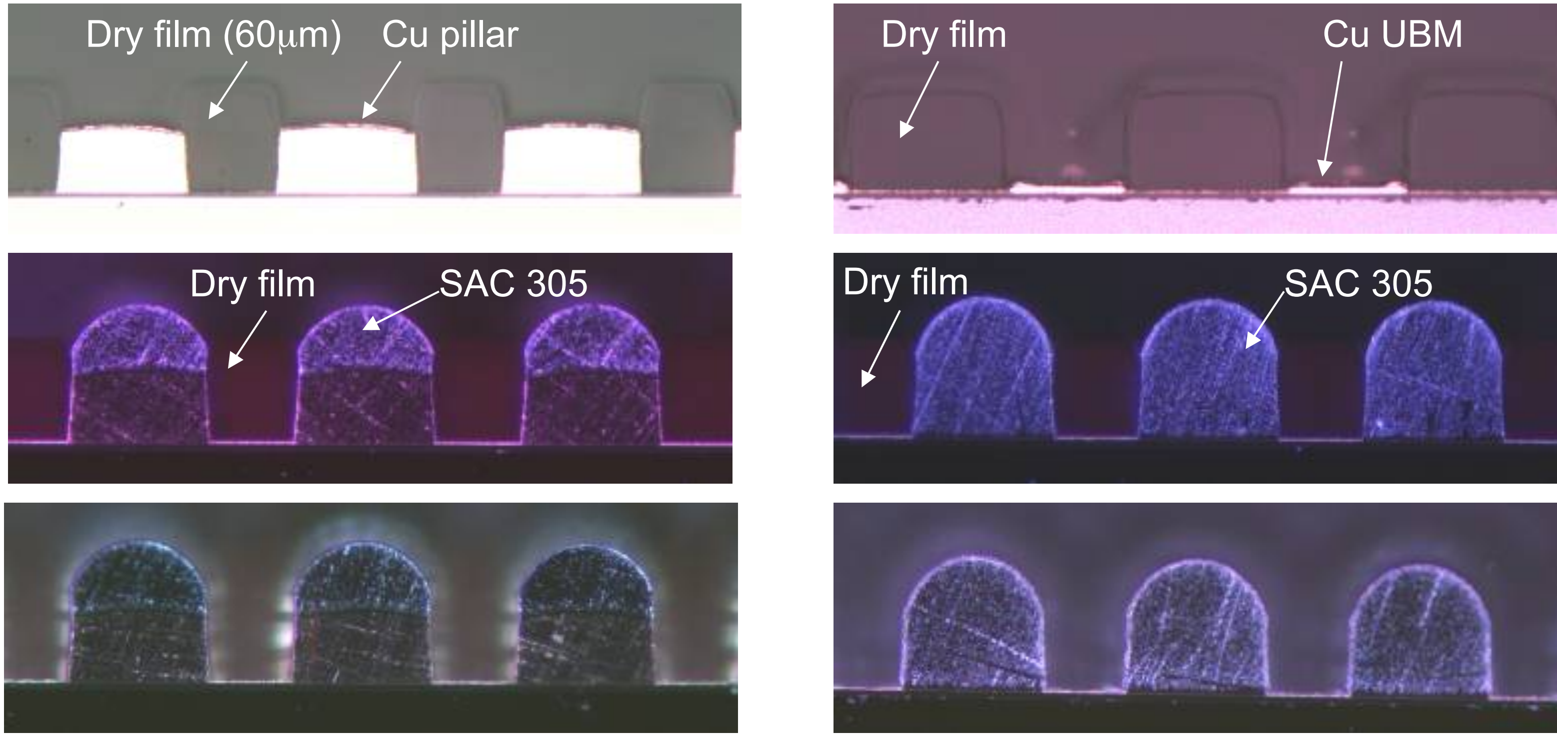
• 40μm thick Cu pillar

• 2μm thick Cu UBM

As received

After IMS

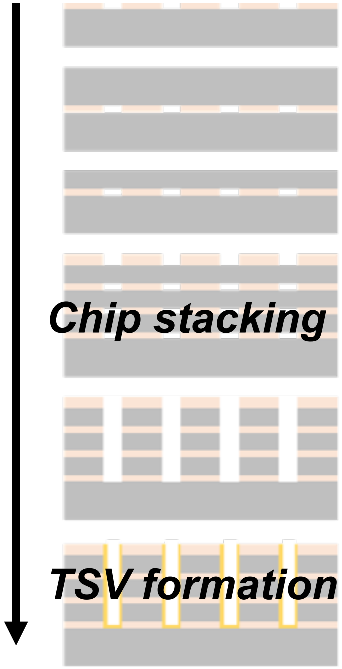
After stripping dry film

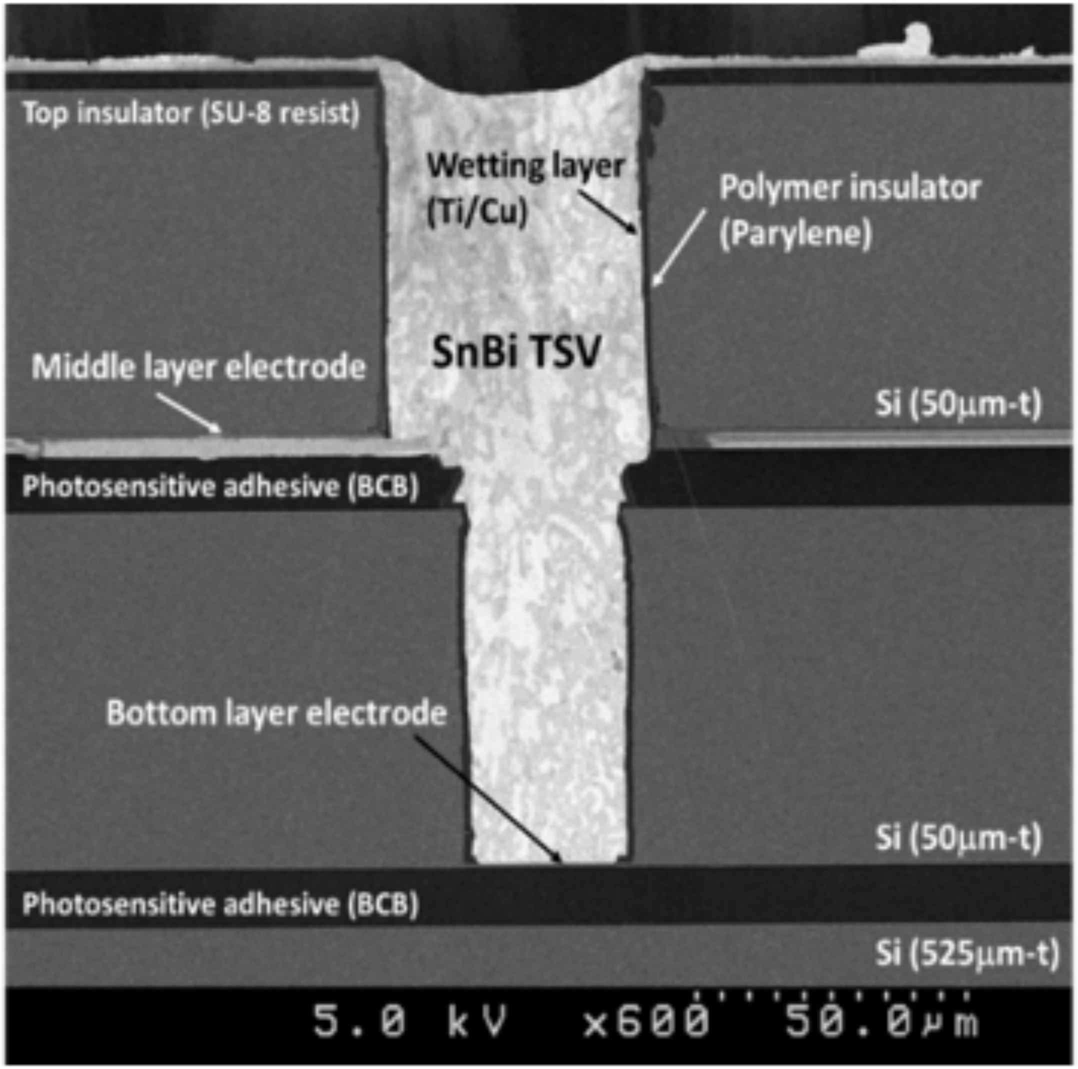


- Particular geometry achieved is unique in industry.
  Straight sidewalls w/ round top of the solder bump on pillar
  → No need additional reflow. It should help with fine pitch.
- Molten solder injection w/o flux → No voids in solders.
- Ability to control solder composition readily.
- No change in throughput even though solder volume increased.

Advanced TSV technology

- Vertical integration after Stacking (ViaS)





A SEM image of ViaS structure

Source: A. Horibe, IBM Japan, ECTC 2015

Thank you for your kind attention!